BEAMCAL FRONT-END ELECTRONICS: DESIGN AND SIMULATION

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The BeamCal specifications for rate, gain, power dissipation, resolution and occupancy set unique challenges in the front-end and readout electronics design. In order to meet the required signal-to-noise ratio, a quasi-triangular weighting function is implemented using a switched-capacitor filter and a slow reset technique. In this context, this paper describes the front-end design procedure and presents SPICE simulation results.
Key words: Front-End Electronics, Switched-Capacitor Circuits, Weighting Function

INTRODUCTION

The BeamCal detector, a calorimeter for the ILC very forward region, has two main purposes: extend the calorimeter hermeticity to small angles, and to provide a fast feedback signal for beam diagnostics and tuning. Very high occupancy is expected, so the data for all bunch crossing must be recorded (no data sparsification). The required resolution is 10 bits, and the maximum input charge is about 36 pC. Bunch crossings occur every 308 ns during almost 1 ms, followed by 199 event-free milliseconds. This cyclic operation is repeated indefinitely. The circuit must have a high sensitivity mode for sensor calibration purposes, with a gain 50x higher than that for science operation. This combination of specifications makes the front-end (FE) design an interesting challenge, because of the large input dynamic range, different modes of operation, rate and data storage.

The most important decisions in a front-end design are usually driven by noise and power consumption specifications [1]. When the input signal rate is limited, it is possible to implement a time-invariant shaper, which can be easily optimized by means of frequency-domain analyses using standard noise models. When the input signal rate is an issue, a time-variant filter is necessary, and its design requires time-domain calculations [2]. In order to have an appropriate weighting function, necessary for an adequate noise performance, correlated double sampling or slow reset techniques are used in time-variant filters.

Considering the peculiar set of specifications for the BeamCal front-end IC, an unusual approach was used to face the electronics design problem. The most important differences from previous works are: the use of g_m/I_D technique for noise analysis, the use of switched-capacitor circuits for the synthesis of an adequate weighting function to take advantage of the total time available for signal processing, and the use of digital data storage. This paper shows the front-end design process, from a system-level perspective to circuit-level details.

THE FRONT-END SYSTEM-LEVEL DESIGN

As mentioned earlier, most decisions in FE designs involve noise, and this is also true in this IC for calibration mode. The total noise power budget was set at $2.75 \cdot Q_n^2$, where Q_n is the quantization noise of a 10-bit analog-to-digital converter (ADC). This is equivalent to an RMS noise of 0.48 LSB for the entire signal path. Considering typical noise performances for each block, the $2.75 \cdot Q_n^2$ noise budget was distributed among the signal path components; particularly, the front-end noise due to charge-sensitive amplifier (CSA) and detector was limited to $1 \cdot Q_n^2$, this is, an equivalent of about 70k electrons for science operation, and 1400 electrons for calibration mode.

In order to assess the noise behavior, with design purposes in mind, a precise noise analysis methodology was developed. The methodology is an extension of the g_m/I_D technique [3], based in the fact that all transistors of the same channel length and same current density present the same transconductance efficiency (g_m/I_D), transit frequency (f_T) and capacitances per unit length. The authors found that this methodology, consequence of simple mathematics on transistors in parallel, can also be extended to noise analysis after a simple normalization step: for all noise models considered, including all BSIM3 model equations [4], the transistor input-referred thermal and flicker noise power spectral densities, multiplied by the device current, are only dependent on g_m/I_D, the channel length and, to some extent, to the drain-to-source voltage. Once this normalization step is done, SPICE computes noise – as well as all other small-signal numbers in any transistor – using the most sophisticated models available, which are unsuitable for simple hand analysis; the results, stored in lookup tables and charts, are adequate for design purposes.

Preliminary noise estimations using the methodology mentioned before helped to find an adequate architecture for the IC. A CSA is the front-end spear, connected to the detector through a coupling capacitor. A 0.8-pF feedback capacitor, used for calibration mode, is permanently connected to the charge amplifier, and a 35.2-pF capacitor is added in parallel for science operation. The CSA closed-loop frequency response acts as a first barrier against noise.

Baseline restoration in 308 ns is best achieved if active, gated reset is used on the CSA; therefore, a time-variant front-end is being considered. For this kind of systems, when properly designed, noise is mostly determined by the front-end weighting function. In this case, the g_m/I_D methodology was used to extract information on thermal and flicker noise coefficients for the most relevant transistors in terms of noise; this information was used in design scripts to obtain an adequate front-end. As a result, the CSA input device current was set at 350 μA, and its g_m/I_D at 17mS/mA.

For science operation, it was found that the expected CSA closed-loop bandwidth suffices for reducing the thermal noise to negligible values, whereas the reset action limits the flicker noise components.

For calibration operation, the weighting function must be carefully tailored in order to maintain noise within adequate values. In fact, for the noise coefficients implied by the CSA design, a perfectly triangular weighting function yields about 700 electrons (RMS) of noise – mainly due to series noise, considering the short processing time – and any departure from an isosceles triangle implies more noise, mainly depending upon the weighting function slope.

In this gated-reset system, the weighting function has two slopes: one due to the direct filter action on the input signal (filter slope), and the other due to the reset action (reset slope). In general, the ideal filter slope for a triangular weighting function can be accomplished by using a perfect integrator with an adequate gain, and the reset slope can be synthesized by means of correlated double sampling (CDS). Considering process-voltage-temperature (PVT) variations of current IC technologies, trapezoidal weighting functions [5] represent a more practical solution, as the weighting function slopes cannot be precisely defined when they depend on high tolerance constants such as RC or g_m/C.

In this chip, the short interval between events implies very limited integration time, and therefore, high sensitivity to series noise components. In order to take advantage of the entire time interval, precision switched capacitor (SC) circuits will be used.

Switched capacitor circuits [6] are sampled data, analog circuits; although the output variable is a continuous voltage, it is only valid in discrete times. As sampling operation is involved, an anti-alias filter is necessary to attenuate out-of-band signals. In SC circuits, resistors are simulated using switched capacitors; therefore, time constants and gains are defined by the ratio of two capacitors and are considerably less sensitive to PVT variations than as RC or g_m/C techniques.

For an adequate synthesis of the weighting function, the filter slope will be defined by the action of a SC integrator; in this case, the CSA closed-loop dominant pole provides the adequate anti-alias filtering action.

The reset slope requires a more careful approach. The CDS technique basically mirrors the filter slope into the reset slope; however, requires additional circuitry to subtract the signal sampled at two different moments. A different approach, based on slowing down the CSA reset action, can be used instead. Specifically, the reset action is engaged as quickly as possible, to allow the CSA to *forget* whatever signal was measured in the previous period; after that, the reset action is slowly released, in order to mitigate the effect of a split doublet. This effectively limits the weighting function's reset slope and also reduces the effect of charge injection, inherent of any MOSFET switch.

In order to achieve a controlled reset-release action, a SC network was designed to gradually reduce the gate-to-source voltage of the reset switch. In other words, the switch transistor's V_{gs} is held by a capacitor during the reset time, and then discharged through a SC resistance during the reset release time. Although this slow reset action produces a weighting function slope far from ideal, it is sufficient for noise filtering.

The switching frequency in a SC circuit is a critical decision in the circuit design. A low switching frequency implies more aliasing and possibly more noise if the anti-alias filter is not well designed; on the other hand, a higher switching frequency requires a faster, power hungry amplifier. A good tradeoff in this design is achieved if the whole period between bunches is sampled a total of 16 times, implying a switching frequency close to 52 MHz. This means 8 periods for integration and 8 periods for reset.

Based on previous considerations, a simplified block diagram for the IC front-end is presented in Fig. 1, where two different signal paths can be found. In normal operation, the ADC reads the voltage directly from the CSA output (lower path), whereas in calibration mode, the switched capacitor integrator is used for filtering purposes (upper path). In this mode, a buffer is required in order to desensitize the CSA operation to large surge currents required by the switched capacitor integrator. In both modes of operation, a slow reset action is implemented for an adequate weighting function. The weighting functions expected from this front-end, considering ideal components, are shown in Figs. 2 and 3.

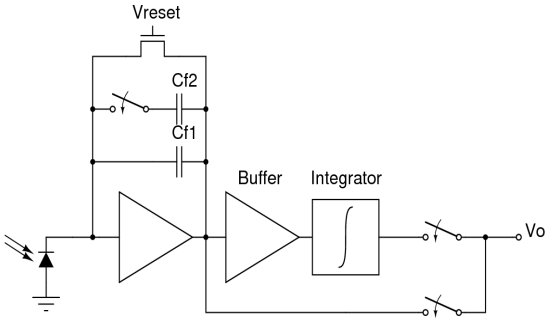

Figure 1. Simplified front-end block diagram, single channel.

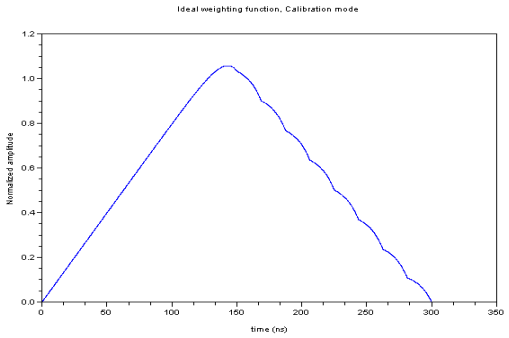

Figure 2. FE weighting function assuming ideal components, calibration mode.

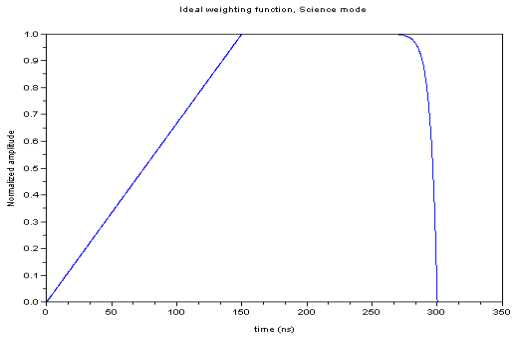

Figure 3. FE weighting function assuming ideal components, science mode.

FRONT-END CIRCUIT IMPLEMENTATION

The circuit presented in previous section consists of a CSA with a built-in slow reset action, a buffer and a switched-capacitor integrator. This section shows the details of each circuit. For PSR and crosstalk considerations, a pseudo-differential architecture is considered in the CSA, followed by fully-differential circuits.

1) Charge-Sensitive Amplifier

A single-ended, folded-cascode topology was chosen due to performance, simplicity and noise considerations (Fig. 4). The polarity is based on NMOS amplifying device (M1), arbitrarily assuming that the detector will consist of common-anode photodiodes; if in the final detector the photodiodes share the cathode terminal instead, the polarity of the CSA will be updated accordingly in following revisions.

In this topology, when properly designed, the main noise contributors are the input and folding transistors (M1 and M4); in fact, both appear in parallel in noise analyses. As mentioned earlier, from noise and performance considerations, the input transistor current was set at 350 □A, and its g_m/I_D at 17mS/mA. Higher transconductance efficiency leads to a more power efficient design; however, it would considerably degrade the slew rate performance in the case of science operation, where the total feedback capacitance is 36 pF.

The amplifier's simulated static gain is 82.6dB, and its open-loop bandwidth is 303 kHz; its input capacitance is 1.1 pF and its output range, arbitrarily defined as the output voltage for less than 40% decrease in static gain, is between 0.22 V and 1.28 V.

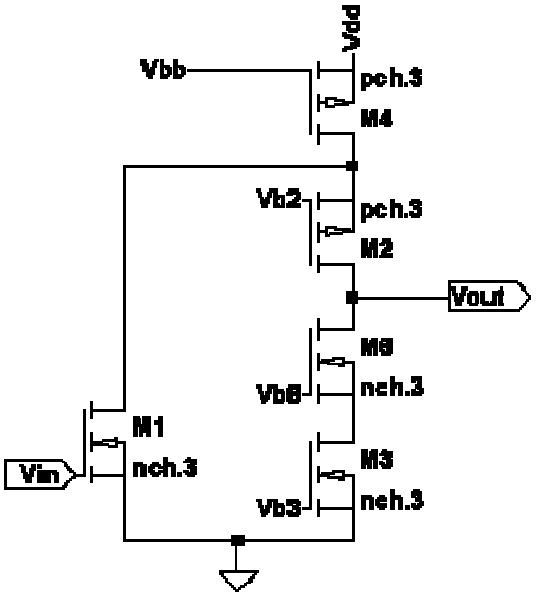

Figure 4. Charge amplifier schematic.

A 0.8-pF feedback capacitor (Cf1) is permanently connected to the CSA; the 35.2-pF feedback capacitor for science operation (Cf2) is switched in and out by means of an NMOS switch, appropriately sized so that the parasitic zero associated with it is far from the CSA closed-loop bandwidth.

The reset switches are sized to allow a fast reset action. As explained earlier, the gate-to-source voltages in these switches are gradually decreased to achieve the slow reset action, by means of the switched capacitor network shown in Fig. 5. The operation of this network requires a two-phase, non-overlapping clock. During □1, C3 shares its initial charge with C4, reducing its voltage by 15%; during□2, the charge in C4 is reset, allowing the cycle to start again.

In order to increase the CSA output range in calibration mode, where its behavior is most sensitive to the open loop gain, the CSA output

voltage must remain within the operational output range. A precharge circuit will be used to achieve this purpose, taking advantage of the circuits necessary for electronics calibration (not shown in this paper). The precharge circuit shifts the CSA reset voltage from the NMOS threshold voltage V_t (approximately 0.5V) down to 0.25V, allowing an output swing of 1V out of a 1.8-V supply.

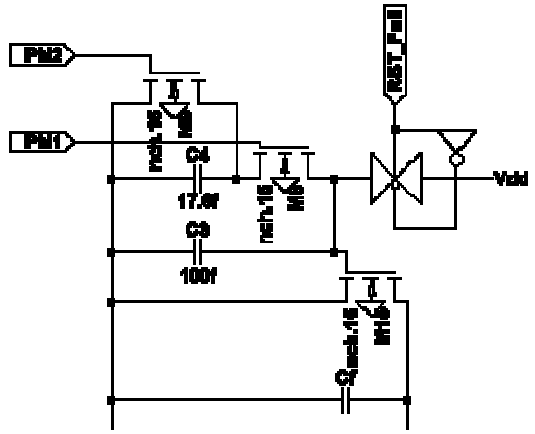

Figure 5. CSA reset circuitry.

2) Buffer

The buffer must replicate the CSA output and desensitize its operation to the rapidly changing capacitive load placed by the switched-capacitor integrator. A practical solution can be found in a source follower (Fig. 6). In this circuit, two important problems must be solved: linearity and input range.

To improve linearity, a PMOS device with body and source tied together (M1) will be used; this configuration is roughly insensitive to body effect. To reduce the current variations that affect linearity, a cascoded current source (M2, M5) is used; to reduce the variations in V_{ds}, a bootstrapping technique [7] is implemented (M3).

The input range of an ideal PMOS-based source follower is between 0 V (actually, less than that if negative voltages are allowed) and V_{dd}-$|V_t|$, approximately 1.3 V in this technology. However, linearity is considerably degraded when operating near the upper limit, thus the performance would benefit from voltage levels lower than those provided by the charge amplifier, even considering precharge. In order to achieve this, a switched capacitor voltage shifting network is implemented (C1 + transmission gates). The network is controlled by two non-overlapping clock signals, RST and RST_b.

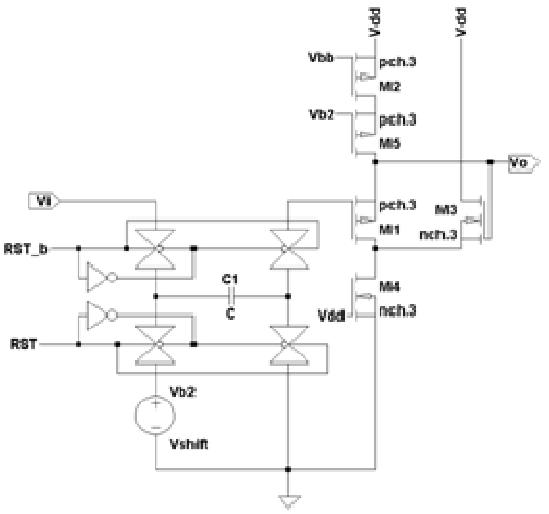

Figure 6. Simplified buffer schematic.

3) Switched-Capacitor Integrator

A simple, fully differential switched-capacitor integrator based on a forward-Euler integration (FEI) algorithm was implemented [6] (Fig. 7). This circuit was preferred over the backward-Euler integration (BEI) due to the fact that represents a lighter load for the driving network.

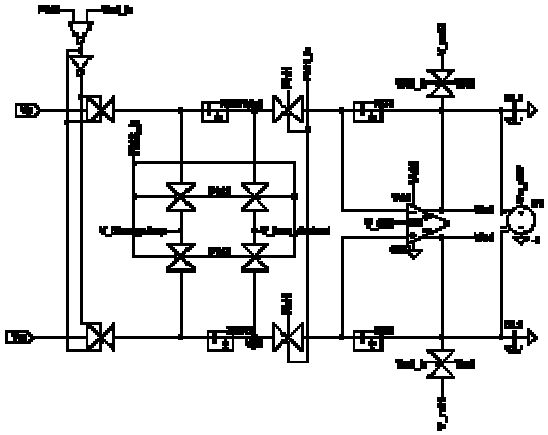

Figure 7. Switched-capacitor integrator schematic.

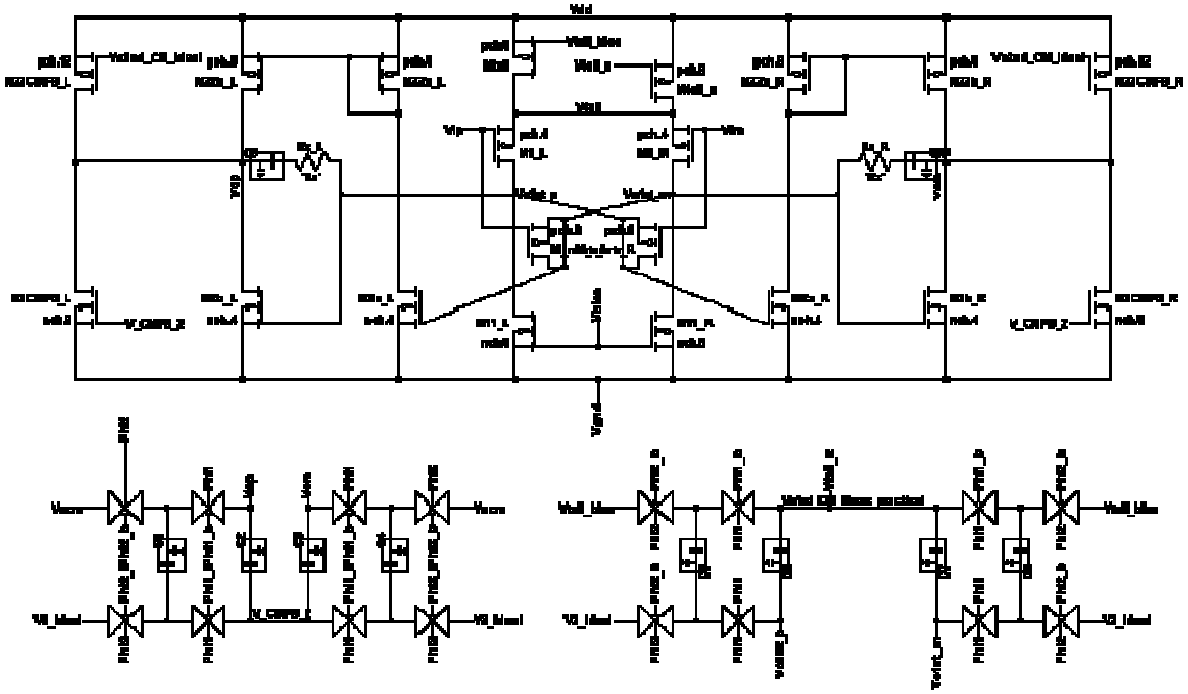

Figure 8. Integrator OTA schematic.

Noise in the integrator comes from two main sources: KT/C noise of all switched capacitors, and amplifier voltage noise. The noise budget allocated for each of these components is $Q_n^2/4$. This figure, along with the switching frequency, sets the lower limit for the integrator capacitor values: 600fF for the feedback capacitors (XC1, XC2), and 150fF for the series, switched capacitors (XCR1, XCR2).

The integrator core is a fully differential, two-stage operational transconductance amplifier (OTA), based in the class A/AB topology presented by Rabii *et al.* [8] (Fig. 8). Class AB output was chosen for power efficiency considerations and the necessity to drive the integrator and load capacitors. For speed vs. power consumption considerations, the second stage is based on NMOS amplifying devices (M2a_R, M2b_R, M2a_L and M2b_L); for adequate common mode range in the internal nodes, the input stage is based on PMOS devices (M1_R and M1_L). At the input, the reset voltages are appropriately set to allow the PMOS input stage to cope with the buffer output voltage levels. Compensation scheme is based on a Miller approach (C9 and C10) with nulling resistor (RZ_R and RZ_L). Class AB output is achieved in a push-pull configuration (M2b_R + M22b_R and M2b_L + M22b_L), and the second stage's quiescent current is set by the first stage output common mode. Each stage requires a common mode feedback network, and both are implemented using switched capacitor circuits, shown at the bottom of the schematic.

SPICE SIMULATIONS

Fig. 9 shows the CSA open loop frequency response, and Fig. 10 presents the front-end output waveforms for calibration mode, for input signals of different amplitudes. Fig. 11 and 12 show the obtained weighting functions for calibration and science modes, respectively.

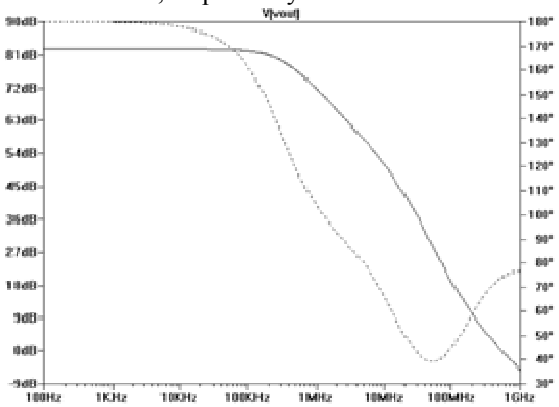

Figure 9. CSA frequency response in magnitude (solid line) and phase (dashed line).

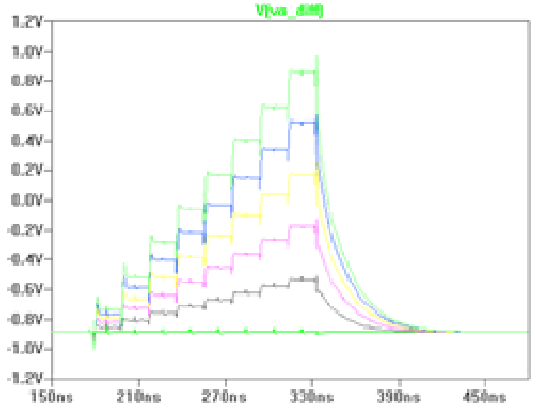

Figure 10. Front-end output waveforms for calibration operation.

Front-end noise computations due to charge amplifier noise yield 6166 electrons for science operation and 1163 electrons for calibration, both below the specified noise budget.

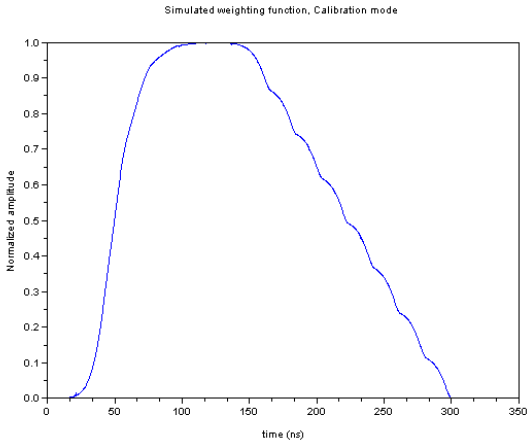

Figure 11. Simulated weighting function for calibration mode.

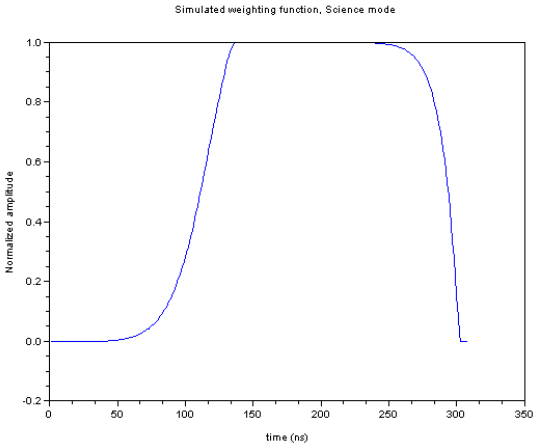

Figure 12. Simulated weighting function for science mode.

CONCLUSION

The circuit-level design process of the BeamCal instrumentation IC's front-end has been presented. A time-variant pulse shaping approach is considered, and the weighting functions are defined using precision switched-capacitor circuits. The time constants involved in the weighting functions are precisely defined, allowing using the complete 308 ns period for signal processing. The additional noise introduced by the finite switching frequency has been assessed and is tolerable in this application.

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