Mismatch of lateral field metal-oxide-metal capacitors in 180 nm CMOS process

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Metal-oxide-metal (MOM) capacitors represent an attractive alternative to metal-insulator-metal (MIM) capacitors in mixed-signal integrated circuits. Since they are made of metal lines, they can be integrated in standard CMOS processes, and tailored over a wide range of sizes. Mismatch data of MOM capacitors, however, is scarce and typically conservative. Presented is the design and the test results of a custom ADC that employs an array of 1024 MOM capacitors sized at 2 fF. Static performance metrics are presented and compared with those for an ADC based on MIM capacitors. Mismatch data is computed from the results.

Introduction: Lateral field, metal-oxide-metal (MOM) capacitors are implemented using the parasitic capacitance between two conductors on a metal layer. Although not as dense as vertical field, metal-insulator-metal (MIM) capacitors when per-layer capacitance is considered, MOM capacitors can be stacked in several metal layers, taking advantage of both the lateral and vertical fields, producing structures with higher capacitance per unit area than that of MIM capacitors. Some foundries are currently providing circuit models for MOM capacitors, marketed from a capacitance density perspective and focused on RF CMOS circuits.

MOM capacitors can also be leveraged from a minimum capacitance perspective. Unlike MIM capacitors, with minimum sizes defined by the foundry through design rules in order to guarantee predictable yield and matching characteristics, the minimum size of MOM capacitors is defined by the interconnect dielectric and by the simplest design rules of the process: wire length and spacing. Therefore, the smallest MOM capacitance that can be fabricated is considerably smaller than the smallest MIM capacitance, and this can lead to the design of lower power circuits [1, 2].

This Letter presents the design and the test results on the mismatch of 2 fF MOM capacitors integrated on a 180 nm standard CMOS process. The capacitors were used in the charge redistribution capacitor array of a successive-approximation-register (SAR) analogue-to-digital converter (ADC).

Design: A custom 10-bit, fully differential 4.3MS/s SAR ADC (similar to the one described in [3]) was designed in a 180 nm standard CMOS process. The converter uses two arrays of 1024 unit capacitors C_u, each implemented with a MOM structure targeting $C_u = 2$ fF per layer. The switched capacitor array, segmented into binary-weighted capacitors for the five LSBs ($2^0 \times C_u$ through $2^4 \times C_u$) and thermometer-coded capacitors for the five MSBs (31 capacitors of size $2^5 \times C_u$), is the core of the internal DAC that makes the successive approximation search possible. This 5-bit/5-bit segmentation described represents a balanced compromise between linearity and simplicity, since it reduces the resulting ADC differential nonlinearity (DNL) standard deviation by 75% from that of a 10-bit binary array, with the only additional requirement of a 5-bit binary-to-thermometer decoder. Fig. 1 presents a simplified schematic of the ADC, where the logic circuits have been omitted.

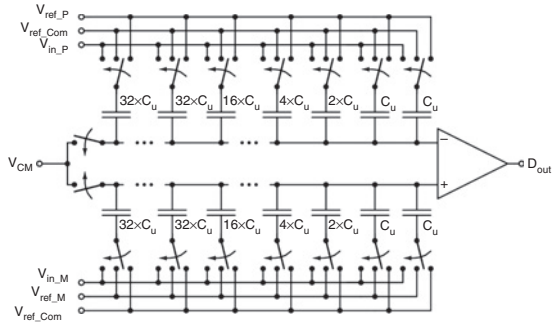

Fig. 1 *Simplified schematic of ADC*

All capacitors were implemented through a parallel connection of unit capacitors, and scattered over the 32 × 32 array on a common-centroid fashion [4] in order to reduce the effects of longitudinal process gradients on the ADC linearity. The array was surrounded by two rows of dummy capacitors, intended to reduce the effects of edge conditions. The unit capacitor design was validated using the Space 3D layout-to-circuit extractor software [5]. Fig. 2 shows a three-dimensional representation of a portion of the capacitor array layout. The specific capacitance estimation is 0.12fF/μm^2-layer, for a 2.9 μm horizontal pitch and a 5.8 μm vertical pitch. The capacitor outer plates are connected together creating the common node in the array, thus reducing the node resistance.

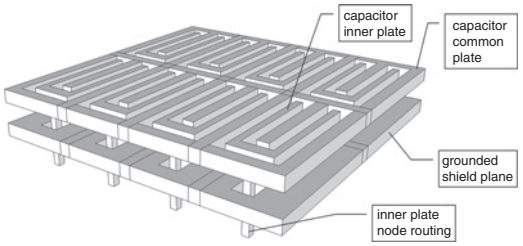

Fig. 2 *Three-dimensional view of portion of single-layer MOM capacitor array, with top shielding layer omitted*

To preserve the linearity of the array, the capacitors were shielded to prevent parasitic field lines from adding an undesired component to any capacitor. Grounded metal planes on the top and bottom of the entire array act as EM shields. Holes in the bottom shield allow routing the inner plate nodes to the ADC switches. Without the shielding planes, there would be an additional capacitive coupling between the long lines that connect the inner plates to the switches and the capacitor array's large common node, affecting the array linearity. The shields increase the capacitance between all the array nodes and ground, but these parasitic capacitances do not affect linearity.

Three converters were integrated: a two-layer MOMCap ADC, a one-layer MOMCap ADC, and a MIMCap ADC using 16 fF unit capacitors made of a vertical-field MIM structure. The results for linearity tests are shown in the following Section.

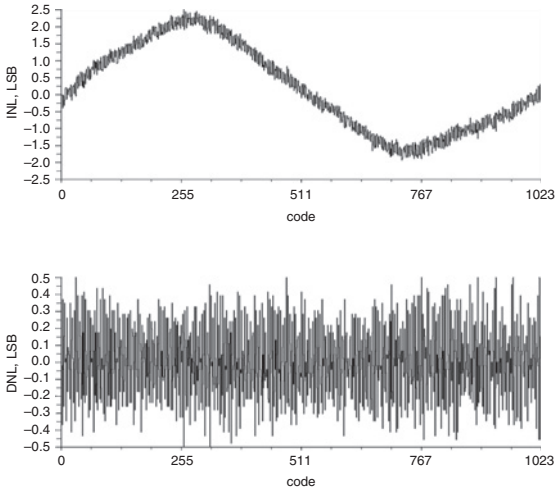

Fig. 3 *Single-layer MOMCap ADC linearity test results*

Test results: The dies were bonded to 44-lead packages and soldered to custom printed circuit boards. The board includes voltage regulators, two AD5541 16-bit DACs to generate the differential input stimuli, and a digital connection to a Digilent Basys2 FPGA evaluation board. The Spartan3e FPGA was programmed to generate a slowly-varying input ramp, and to collect the output data from the DUT. After the output data was checked for monotonicity, the histogram methodology was used in order to compute the ADC's DNL and integral nonlinearity (INL). Table 1 shows a summary of the test results, along with calculations of the unit capacitance mismatch obtained from the measured code widths, expressed as standard deviation. Fig. 3 presents the DNL and INL of the single-layer MOMCap ADC. The DNL shows no missing codes, whereas the INL exhibits a cubic-like shape. Behavioural simulations show that the cubic-like INL characteristic can be explained as a consequence of the edge effects in the capacitor array, which produced

radial gradients. This can be solved in future revisions by randomising the thermometer-coded capacitor locations in the array, to make it insensitive to radial gradients.

Table 1: Summary of ADC linearity test results

ADC	Specific capacitance ($fF/\mu m^2$)	INL_{max}/INL_{min} (LSB)	DNL_{max}/DNL_{min} (LSB)	Unit capacitance mismatch (Std. Dev.)
MIMCaps ($C_u = 16fF$)	1	0.61/ − 0.77	0.16/ − 0.17	2.4%
Two-layer MOMCaps ($C_u = 4fF$)	0.24	1.7/ − 1.2	0.29/ − 0.24	5.5%
One-layer MOMCaps ($C_u = 2fF$)	0.12	2.5/ − 1.9	0.55/ − 0.56	9.2%

The Pelgrom mismatch coefficients [6] were computed from the data, resulting in 9.6%-μm for the MIM capacitor (with a specific capacitance of 1 $fF/\mu m^2$), and 34.9%-μm-$\sqrt{N_{layer}}$ for the MOM capacitors (with a specific capacitance of 0.12 $fF/\mu m^2$-layer), where N_{layer} is the number of layers of MOM capacitors. It draws attention to the ratio of the mismatch coefficients between MIM and MOM capacitors; however, when specific capacitance is considered, the coefficients become only 25% apart. That difference comes from the nature of the capacitors: MIM capacitor plates are shaped through photolithography and spaced through deposition, whereas MOM capacitor plates are shaped and spaced in the opposite way.

Conclusion: The mismatch of MOM capacitors in a 180 nm standard CMOS process has been estimated by means of linearity tests on a custom 10-bit SAR ADC. The data obtained allows designing linear, power- and area-efficient capacitor arrays made of integrated metal lines, fully compatible with any CMOS process. The small size of the capacitor array results in a low load for the ADC input voltage and internal switch drivers. Combined with a power-efficient comparator, it is possible to design very low power, medium-speed, medium-resolution ADCs compatible with wireless sensor networks.

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