Noise power normalisation: extension of g_m/I_D technique for noise analysis

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MOSFET models for deep submicron technologies involve accurate and complex equations not suitable for hand analysis. Although the g_m/I_D design-oriented approach has overcome this limitation by combining hand calculations with data obtained from SPICE simulations, it has not been systematically used for noise calculations, since the dependence of noise on this parameter is not direct. An attempt to express noise as a function of g_m/I_D is presented. By introducing the normalised noise concept, noise curves that depend solely on the device length and operation point can be obtained directly from SPICE simulations, and then used in the design flow. The main outcome is a simple design-oriented methodology for noise calculations that does not depend on equations for a specific technology or operating region, and that is easy to migrate among different technologies.

Introduction: The evolution of MOSFET models for deep submicron technologies has improved the accuracy of SPICE simulation results. However, the equations have become non-practical for hand calculations, and the use of simple equations leads to inaccurate results. Although the g_m/I_D methodology overcomes this limitation using accurate SPICE simulation results as data for hand analysis [1, 2], this methodology does not state clearly how to deal with noise analysis. An application for the use of the g_m/I_D methodology for noise analysis was later developed [3], but the procedure relies on extracting two noise parameters instead of a detailed curve of noise over frequency, and does not provide an insight into the dependence of noise on the g_m/I_D parameter. A new noise analysis technique, presented in this Letter, attempts to overcome this limitation. Noise curves for a set of transistors are pre-computed by means of SPICE simulations, using the most comprehensive noise models available. The curves are then properly scaled for the appropriate device parameters using the g_m/I_D technique, conveniently modified in this work to include noise. Finally, noise can be computed by using simple interpolations within the curves.

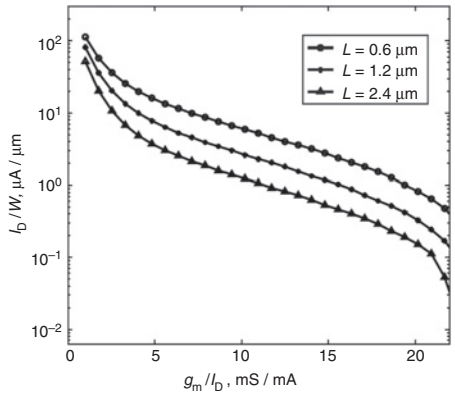

Fig. 1 *I_D/W against g_m/I_D for different transistor lengths*

To ensure that device is biased in saturation region, simulations done with $V_{DS} = V_{GS}$

g_m/I_D basics: Consider a transistor biased at a certain operation point, with a drain current I_D and an overdrive voltage V_{OV}. If another transistor with the same parameters and bias is connected in parallel, the compound transistor will have the following variables doubled in magnitude: drain current (I_D), effective width (W), gate-to-source capacitance (C_{gs}) and transconductance (g_m). The overdrive voltage V_{OV} and the level of inversion in the channel remain unchanged. The ratio g_m/I_D also remains constant, and is a measure of the operation point of the transistor. Large values of g_m/I_D are related to subthreshold and weak inversion operation (low overdrive voltage), whereas small values are related to strong inversion operation (high overdrive voltage). It can be shown that the transconductance efficiency is $g_m/I_D = 2/V_{OV}$ in strong inversion, and $g_m/I_D = q/nk_BT$ in weak inversion, where q is the electron charge, n is a dimensionless parameter, k_B is the Boltzmann constant and T is the absolute temperature [4]. Other ratios that can be mapped to the operation point are the transistor transit frequency f_T, usually defined as g_m/C_{gs}, and the current density I_D/W. As an example, Fig. 1 shows the dependence of I_D/W on g_m/I_D for different transistor lengths for an NMOS device in a 0.6 µm technology, obtained via SPICE simulations. Likewise, sets of curves such as C_{gs}/W, f_T, V_{th} and V_{OV} as functions of g_m/I_D can be easily obtained for any technology. Unfortunately, the transistor noise does not depend directly on g_m/I_D, thus the corresponding curves cannot be represented in this fashion.

Normalised noise power: As mentioned earlier, when two transistors in the same bias condition are connected in parallel, g_m/I_D remains constant, but the drain current noise power (I_n^2) is doubled. If we want to reach a noise quantity that does not vary when g_m/I_D remains constant, we need to divide the drain current noise power by any quantity that is doubled in the compound transistor, e.g. by I_D, g_m or W. Thus, MOSFET noise can be expressed as a function of g_m/I_D by doing a simple normalisation, this is, by dividing the transistor drain current noise power spectral density by the drain current. For a certain channel length and operation point, the normalised noise power spectral density ($\hat{I}_n^2$) depends only on the technology, and can be easily obtained from SPICE simulations using models with arbitrary complexity. Later in a circuit design stage, lookup tables allow retrieving the required values for denormalisation, to be used in simple hand calculations. The noise power referred to the transistor gate voltage (V_n^2) can also be normalised ($\hat{V}_n^2$) by multiplying it by the drain current, and can also be obtained by dividing $\hat{I}_n^2$ by $(g_m/I_D)^2$.

The dependence of the normalised noise on g_m/I_D has been confirmed for different noise equations that model thermal, shot and flicker noise, including the equations used in the BSIM3v3 models. Table 1 presents examples of simple noise equations used by some SPICE models and their normalised versions [5, 6]. Even though flicker noise can be further explained by several processes and modelled accordingly [7, 8], this work aims to provide a design-oriented methodology for which the specific models used are not relevant, so the circuit designer does not have to deal with the complexity of the equations.

Table 1: Normalised noise equations, where k_B is Boltzmann constant, T is temperature, γ is thermal coefficient, q is electron charge, and K_F and A_F are flicker noise parameters

	I_n^2	$\hat{I}_n^2$
Thermal noise	$4 \times k_B \times T \times \gamma \times g_m$	$4 \times k_B \times T \times \gamma \times (g_m/I_D)$
Shot noise	$2 \times q \times I_D$	$2 \times q$
Flicker noise	$\frac{K_F \times g_m^2}{C_{OX} \times W \times L \times f^{A_F}}$	$\frac{K_F \times (g_m/I_D)^2}{C_{OX} \times (W/I_D) \times L \times f^{A_F}}$

Fig. 2 shows $\hat{V}_n^2$ for different values of g_m/I_D. The spectra present a low-frequency region dominated by the flicker noise, and a high-frequency region dominated by thermal or shot noise, depending on the inversion level of the device. Low values of g_m/I_D imply large values of the corner frequency, f_c, which corresponds to the frequency at which the white and $1/f$ components of noise are equal. This is because when g_m/I_D decreases, as shown in Fig. 1, the I_D/W ratio increases and, for constant bias current, W decreases; as a consequence of a reduced gate area, flicker noise dominance extends to higher frequencies.

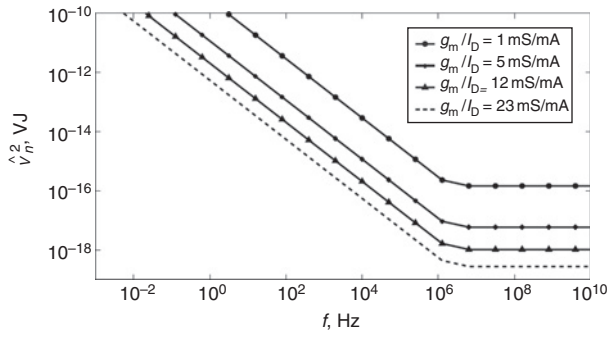

Fig. 2 *Normalised noise against frequency for different values of g_m/I_D and $L = 0.6$ µm*

Normalised noise provides an intuitive interpretation of noise representing it as a function of g_m/I_D and the frequency, and can be easily extended to represent more complex noise models, such as those that depend on the drain-to-source voltage.

Conclusions: A method for noise analysis based on an extension of the g_m/I_D design-oriented technique has been presented. With this method, noise analysis can be carried out without the need of complex equations for each noise process. Instead, different noise processes that behave differently over frequency are treated as a whole from a behavioural point of view. The methodology is adequate for design-oriented analysis and provides a better insight into the design trade-offs for the transistor operation point, via the g_m/I_D technique and the normalised noise concept. The methodology presented also allows an accurate noise analysis in all the transistor operation regions, and is easy to migrate among different technologies.

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