Fully-Differential Offset-Cancelling Circuit with Configurable Output Common-Mode Voltage

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***Abstract*— For certain applications, the offset voltage of the amplifiers represents a problem that must be addressed, since it may affect the transfer characteristics of the system. Offset memorization techniques allow to partially cancel the offset voltage either at the input or at the output of an amplifier, but their effectiveness is highly dependent on the amplifier gain. For this reason, these techniques do not result in a complete offset cancellation when used with low-gain amplifiers. In this work, a fully-differential offset-cancelling circuit based on offset memorization techniques is introduced along with its analysis and simulation results. Among the features of the proposed circuit are a configurable output common-mode voltage and a complete offset cancellation even when used with low-gain amplifiers.**

I. Introduction

In electronic amplifiers, the offset voltage is a non-ideality produced by layout asymmetries, process variations, devices mismatch and temperature gradients among other causes. Depending on the application, the offset voltage may have adverse effects on the operation of the circuits in which the amplifiers are used. For example, the linearity of a passive charge-sharing based analog-to-digital converter (ADC) [1] is sensitive to the pre-amplifier and comparator offset voltage, whereas in the classical charge redistribution successive approximation register architecture this voltage only introduces a global offset in the ADC transfer characteristics [2]. The storage techniques [3], [4], also useful to cancel low-frequency noise, aim to partially cancel the offset voltage of an amplifier by storing the offset in a capacitor connected in series with the amplifier input, or alternatively, in series with the amplifier output [5]. For these techniques to work properly, the amplifier gain must be large enough to ensure that the residual offset is negligible and does not affect the overall circuit operation.

In certain applications such as data converters, the offset cancellation is sometimes done offline [6]. These techniques, however, preclude the circuit from being used during the calibration routine, and therefore, pre-amplifiers with offset storage are still required [7].

In this work we present a fully-differential offset-cancelling circuit based on the well-known offset memorization technique, which allows for a configurable output common-mode voltage and provides a total offset cancellation even when used with low-gain amplifiers. The circuit operates in two steps, the first one related to the usual offset storage, and the second one related to the offset subtraction.

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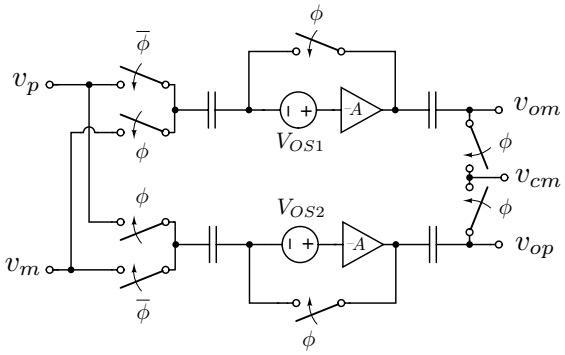

Fig. 1. Fully-Differential offset-cancelling circuit simplified schematic.

The paper is structured as follows: Section II shows the proposed circuit along with its theoretical analysis, in Section III, design considerations and non-idealities are discussed. Then, in Section IV, simulation results are reported, and in Section V, implementation details are given. Finally, in Section VI, the conclusions are drawn.

II. Circuit Design

Fig. 1 shows the simplified schematic of the offset-cancelling circuit, where v_p and v_m are the input voltages, v_{op} and v_{om} are the output voltages, V_{OS1} and V_{OS2} are the amplifiers input-referred offset voltages, A is the gain of each amplifier, v_{cm} is the configurable output common-mode voltage, and ϕ is the control signal. The circuit operates in two steps. At the first step ($\phi = 1$), the amplifiers inputs are short-circuited to their respective outputs, and the input-referred offset voltages are stored in the capacitors. Typically in this phase, which corresponds to the offset memorization step [4], the circuit inputs are connected to ground, but as it will be shown later, swapping the inputs allows to duplicate the gain [8]. At the second step ($\phi = 0$) the amplifiers inputs and outputs are no longer short-circuited, the input capacitors are connected between the input voltages and the amplifiers inputs to partially cancel the offset of each amplifier, and the output capacitors are connected between the amplifiers outputs and the output voltages to subtract the amplified residual offset voltage that was not cancelled by the input capacitors due to the amplifiers finite gain.

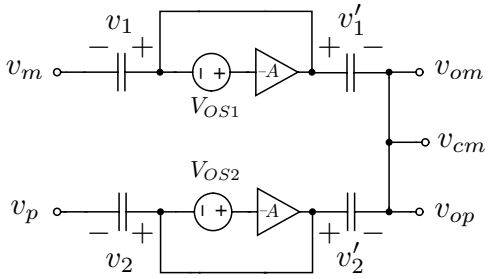

Fig. 2. Equivalent circuit at the first step of operation when the switches controlled by ϕ are closed.

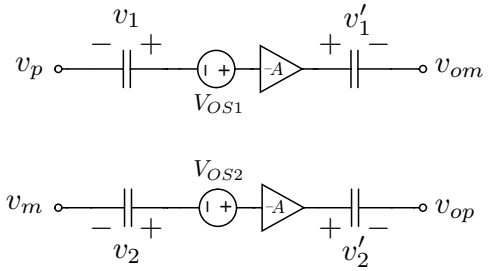

Fig. 3. Equivalent circuit at the second step of operation when the switches controlled by $\bar{\phi}$ are closed.

Fig. 2 shows the equivalent circuit at the first step of operation when the switches controlled by ϕ are closed. From the circuit schematic, voltages v_1, v_1', v_2, v_2' can be computed as

$$v_1 = -\frac{A}{1+A}V_{OS1} - v_m \quad (1)$$

$$v_1' = -\frac{A}{1+A}V_{OS1} - v_{cm} \quad (2)$$

$$v_2 = -\frac{A}{1+A}V_{OS2} - v_p \quad (3)$$

$$v_2' = -\frac{A}{1+A}V_{OS2} - v_{cm}. \quad (4)$$

The equivalent circuit at the second step of operation is depicted in Fig. 3, where voltages v_{op} and v_{om} can be computed as

$$v_{op} = -A(v_m + v_2 + V_{OS2}) - v_2' \quad (5)$$

$$v_{om} = -A(v_p + v_1 + V_{OS1}) - v_1'. \quad (6)$$

After replacing (1), (2), (3) and (4) into (5) and (6), v_{op} and v_{om} can be written as

$$v_{op} = A(v_p - v_m) + v_{cm} \quad (7)$$

$$v_{om} = -A(v_p - v_m) + v_{cm}. \quad (8)$$

Finally, the differential output voltage $v_{od} = v_{op} - v_{om}$ and the common-mode output voltage $v_{ocm} = (v_{op} + v_{om})/2$ are given by

$$v_{od} = 2Av_{id} \quad (9)$$

$$v_{ocm} = v_{cm} \quad (10)$$

where $v_{id} = v_p - v_m$ is the differential input voltage. As shown in (9), the offset voltages V_{OS1} and V_{OS2} are completely subtracted from the signal and do not appear in the expression of v_{od}, and the differential input voltage is amplified by $2A$ instead of A. The circuit operation does not depend on the input common-mode voltage v_{icm}, and the output common-mode voltage v_{ocm} depends solely on the external reference v_{cm}.

Stability considerations in the amplifiers design must take into account that, during $\phi = 1$, the amplifiers are connected in a voltage buffer configuration.

III. Other Considerations

A. Gain Mismatch

Following the deduction of the previous section, but considering that the top branch amplifier gain is given by $A_1 = A$, and the bottom branch amplifier gain is given by $A_2 = A_1(1 + \Delta)$, the differential output voltage v_{od} and the common-mode output voltage v_{ocm} can be calculated as

$$v_{od} = (2 + \Delta)Av_{id} \quad (11)$$

$$v_{ocm} = v_{cm} + \frac{\Delta A}{2}v_{id}. \quad (12)$$

The gain mismatch does not alter the circuit operation, since the offset voltages are still successfully subtracted from the signal. However, the output common mode voltage now depends on v_{id}, and the circuit gain is not exactly doubled as in the ideal-case scenario. In order to decouple v_{ocm} from v_{id}, A_1 and A_2 must be well matched.

B. Capacitor Sizes and Mismatch

Due to the amplifiers input capacitances to ground and the capacitances connected at the amplifiers inputs, there is a capacitive voltage divider at both circuit inputs which is responsible for the attenuation of the input voltages v_p and v_m. In order to prevent an asymmetrical attenuation of the input voltages, the capacitors connected at the amplifiers inputs should be sized equally. As a means to match the circuit output impedances, the capacitors connected at the amplifiers outputs should be well matched too. To determine the capacitor sizes, noise and power/speed constraints should be considered.

C. Noise Analysis

After the first step of operation (see Fig. 2), each capacitor holds a voltage noise power of kT/C, where k is the Boltzmann constant, T is the absolute temperature and C is the capacitance. The circuit input-referred noise can be calculated by adding the kT/C_1 held by the input capacitors, the amplifiers input-referred noise $\overline{v_A}^2$, and the kT/C_2 held by the output capacitors attenuated by the amplifier transfer function squared A^2. Therefore, the total input-referred noise $\overline{v_{in}^2}$ is given by

$$\overline{v_{in}}^2 = 2\overline{v_A}^2 + 2kT\left(\frac{1}{C_1} + \frac{1}{A^2C_2}\right). \quad (13)$$

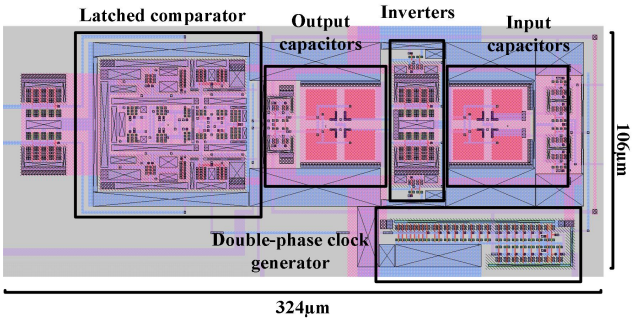

Fig. 4. Fully-differential offset-cancelling circuit and latched comparator layout.

TABLE I

SIMULATED MAXIMUM AND MINIMUM VALUES OF v_{ocm} FOR $v_{cm} = 1,\ 2,\ 3$ AND 4 V.

v_{cm}	Minimum v_{ocm}	Maximum v_{ocm}
1 V	0.93 V (-7%)	1.22 V ($+22\%$)
2 V	1.83 V (-8.5%)	2.12 V ($+6\%$)
3 V	2.77 V (-7.7%)	3.06 V ($+2\%$)
4 V	3.77 V (-5.7%)	4.06 V ($+1.5\%$)

For the deduction of (13) it is assumed that the input capacitors are sized equally and that the output capacitors are sized equally too.

IV. Simulation Results

The proposed circuit was designed for a 0.5-μm technology using CMOS inverters as amplifiers, CMOS switches and 500-fF capacitors[1]. Simulations were carried out using SPICE. Ideal voltage sources were placed in series with each amplifier input to emulate the input-referred offset voltages V_{OS1} and V_{OS2}. To test the circuit an input voltage v_{id} ramp from -0.1 V to 0.1 V was used, and the differential output voltage v_{od} was measured for several offset voltage values from -1 V to 1 V, and several input common-mode voltage v_{icm} values from 0.1 V to 4.9 V. The clock was set at $f = 10$ MHz. The results show that the offset is completely cancelled even for the worst-case scenarios given by $V_{OS1} = \pm 1$ V and $V_{OS2} = -V_{OS1}$.

Table I shows the maximum and minimum values of v_{ocm} obtained from the simulation for four different values of v_{cm}, $V_{OS1} = 1$ V, $V_{OS2} = -1$ V, $v_{icm} = 3$ V, and v_{id} from -0.1 V to 0.1 V. According to (10), the variations of v_{cm} are due to the gain mismatch produced by the mismatch in the amplifiers bias condition, which depends on the input voltages v_p and v_m.

V. Circuit Implementation

The offset-cancelling circuit along with a latched comparator connected at the output was implemented in a 0.5-μm mixed-signal CMOS process. Fig 4 shows the $324 \times 106 \mu\text{m}^2$ circuit layout intended for the use in a data converter, where two CMOS inverters were used as amplifiers. The circuit has not been tested yet.

[1]Generic 0.5-μm transistor models available at MOSIS website [9] were used for this work.

VI. Conclusion

A fully-differential offset-cancelling circuit based on offset memorization techniques was introduced. Simulation results show that the proposed circuit effectively removes the input-referred offset voltage without the need of a high-gain amplifier. Also, the proposed circuit has a configurable output common-mode voltage, duplicates the amplifier gain, and its operation does not depend on the input common-mode voltage. The circuit has been implemented in a 0.5-μm mixed-signal CMOS process, but it has not been tested yet.

Acknowledgment

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